REMARKS

The above amendments and these remarks are responsive to the Office Action issued on March 8, 2005. By this response, claims 1 and 10 are amended. No new matter is added. Claims 1-13 and 15-19 are now active for examination. A petition for a one-month extension of time is submitted concurrently herewith.

The Office Action

The final Office Action dated March 8, 2005 rejected claims 1-13 and 15-18 under 35 U.S.C. §103(a) as being unpatentable over Okado (EP 0511484A2) in view of Hennessy (Computer Architecture). Claim 19 stood rejected under 35 U.S.C. §103(a) as being unpatentable over Okado in view of Hennessy and Watanabe (U.S. Patent No. 5,214,786).

It is respectfully submitted that the rejections are overcome in view of the amendments and/or remarks presented herein.

The Obviousness Rejection Based on Okado and Hennessy Is Traversed

Claims 1-13 and 15-18 were rejected as being unpatentable over Okado in view of Hennessy. The obviousness rejection is respectfully traversed because Okado and Hennessy cannot support a prima facie case of obviousness.

Claim 1, as amended, recites:

> A data processing apparatus comprising:
> an instruction memory...;
> a data memory...
> a memory operation unit...fetching an instruction stored in said instruction memory, and accessing said data memory according to a decode result of said instruction decoder; and
> ...
> said memory operation unit generating a pipeline cycle corresponding to selection of an instruction memory bank to be accessed in a following pipeline cycle and a pipeline cycle corresponding to instruction readout only from said selected instruction memory bank without reading out any instructions from unselected instruction banks to carry out pipeline

processing when a plurality of instructions are fetched from the plurality of instruction memory banks.

Therefore, in an apparatus of claim 1, the memory operation unit generates (1) a pipeline cycle corresponding to selection of an instruction memory bank to be accessed in a **following** pipeline cycle **and** (2) a pipeline cycle corresponding to instruction readout only from said selected instruction memory bank **without** reading out any instructions from unselected instruction banks to carry out pipeline processing when a plurality of instructions are fetched from the plurality of instruction memory banks. Apparently, an instruction is not read out from an unselected bank, and the apparatus performs bank selection and memory reading in a specific order.

In contrast, Okado merely discusses that a repeat controller 207 causes the instruction registers IR1 and IR2 to retain their instructions depending on the occurrence of an internal state requiring particular instructions held in the micro ROM 201 to be executed repeatedly. In doing so, the repeat controller 207 controls the timing generator TG and program counter PC to inhibit access to the micro ROM 201 so that the target instructions for recurrent execution will be output repeatedly from instruction registers IR1 and IR2. See column 9, lines 35-45 of Okado. However, Okado does not each that "said memory operation unit generating a pipeline cycle corresponding to selection of an instruction memory bank to be accessed in a following pipeline cycle and a pipeline cycle corresponding to instruction readout only from said selected instruction memory bank without reading out any instructions from unselected instruction banks to carry out pipeline processing when a plurality of instructions are fetched from the plurality of instruction memory banks," as recited in claim 1.

Hennessy, the other reference relied on by the Office Action, does not alleviate the deficiency of Okado. Although the Hennessy reference arguably performs a bank selection process for data transfer, the bank selection does **not** reduce the number of memory banks that operate

during memory reading. If a synchronized access is performed according to the Hennessy reference, memory reading is conducted in parallel with respect to **all** banks, and bank selection is conducted to transfer data in an order depending upon the bank number subsequent to memory reading. Therefore, a bank selection is **not** conducted before memory reading. In other words, a bank is selected after an instruction is fetched.

Furthermore, in accordance with the example described in the Hennessy reference, the memory is divided into eight banks when 64 double-precision data is to be loaded. All the banks are accessed in parallel to read out eight units of data. Each unit of the data is sequentially selected (bank selection) according to the bank number, whereby eight data transfers are conducted in eight cycles.

On the other hand, an exemplary data processing apparatus according to claim 1 differs from Hennessy in that bank selection, memory reading and data transfer are set in a pipeline manner. This approach is advantageous in that memory power consumption is reduced, by operating only the required memory bank from a plurality of memory banks according to the result of bank selection (for example, only one of eight banks is selected, and only the selected one is operated). In contrast, Hennessy operates **all** the banks and hence power consumption cannot be reduced since memory reading is always conducted for **all** the banks. Accordingly, like Okado, Hennessy also fails to disclose "said memory operation unit generating a pipeline cycle corresponding to selection of an instruction memory bank to be accessed in a **following** pipeline cycle and a pipeline cycle corresponding to instruction readout **only** from said selected instruction memory bank without reading out any instructions from unselected instruction banks to carry out pipeline processing when a plurality of instructions are fetched from the plurality of instruction memory banks," as recited in claim 1.

Thus, Okado and Hennessy, even if combined, do not disclose every limitation of claim 1, and hence cannot support a prima facie case of obviousness. Therefore, the obviousness rejection is untenable and should be withdrawn. Favorable reconsideration of claim 1 is respectfully requested.

Claim 10, like claim 1, describes that "said memory operation unit generates a pipeline cycle corresponding to selection of an instruction memory bank to be accessed in a following pipeline cycle and a pipeline cycle corresponding to instruction readout only from said selected instruction memory bank without reading out any instruction from unselected instruction banks to carry out a pipeline process when fetching an instruction from said plurality of instruction memory banks." As discussed earlier related to claim 1, neither Okado nor Hennessy discloses these features. Consequently, claim 10 is patentable over the combination of Okado and Hennessy. Favorable reconsideration of claim 10 is respectfully requested.

Claims 2-9, 11-13 and 15-18, directly or indirectly, depend on claims 1 and 10, respectively, and incorporate every limitation thereof. Therefore, the obviousness rejection of claims 2-9, 11-13 and 15-18 based on Okado and Hennessy also is untenable and should be withdrawn based on at least the same reasons for claim 1 or 10, as well as based on their own merits. Favorable reconsideration of claims 2-9, 11-13 and 15-18 is respectfully requested.

The Obviousness Rejection Based on Okado, Hennessy and Watanabe Is Overcome

Claim 19 depends on claim 10 and was rejected as being obvious over Okado and Hennessy, and further in view of Watanabe. As pointed out previously, both Okado and Hennessy fail to disclose that "said memory operation unit generating a pipeline cycle corresponding to selection of an instruction memory bank and a pipeline cycle corresponding to instruction readout from said

selected instruction memory bank to carry out pipeline processing when a plurality of instructions are fetched from the plurality of instruction memory banks," as recited in claim 10. Watanabe also fails to teach this feature. Therefore, Okado, Hennessy and Watanabe, even if combined, do not teach every limitation of claim 19 by virtue of its dependence from claim 10. The obviousness rejection based on Okado, Hennessy and Watanabe is untenable and should be withdrawn. Favorable reconsideration of claim 19 is respectfully requested.

For the reasons given above, Applicants believe that this application is conditioned for allowance and Applicants request that the Examiner give the application favorable consideration and permit it to issue as a patent. However, if the Examiner believes that the application can be put in even better condition for allowance, the Examiner is invited to contact Applicants' representatives listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP

Wei-Chen Nicholas Chen
Recognized under 37 CFR §10.9(b)

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 WC:apr
Facsimile: (202) 756-8087
Date: July 8, 2005